Ultralow Current Density RTDs for Tunneling-Based SRAM

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Abstract. We report an improved tunneling-based SRAM (TSRAM) cell design using *symmetric* low current density InGaAs/InAlAs/AlAs/InAs resonant-tunneling diodes (RTDs). The new design eliminates an interconnect compared to the previous record low 50 nW TSRAM cell demonstrated with *asymmetric* low current density RTDs and heterostructure field-effect transistors (HFETs) in our InP-based integrated process. The simplified cell has 4× smaller area than III-V FET-only SRAM cells at the same design rule. We also investigate experimentally and theoretically the mechanism for reduced peak-to-valley current ratios for very low current density (~ 1 A/cm^2) RTDs which affects TSRAM cell standby power.

1. Introduction

High-speed static random access memory (SRAM) is required for fast processors. Although 1M transistor circuits can now be fabricated in III-V technology [1], one of the shortcomings remains the absence of reasonable density low-power on-chip memory. Access times as low as 0.5 ns have been realized for a 4 kbit HFET SRAM [2], but 64 kbit has been the integration limit with 5 W total power dissipation (1.2 ns access [3]). Using familiar circuit design, the n-channel GaAs 6-transistor (6T) cell cannot compete with the complementary Si 6T cell, which consumes less than 1 pW [4]. On the other hand, HFETs have intrinsic advantages for very high speed low power addressing because of the high cutoff frequency f_T at low drain current and good short channel behavior [5]. A low power compound semiconductor memory could enable on-chip data processing for ultrahigh speed chips.

We have recently demonstrated a III-V ultralow standby power (50 nW/bit, compared to about 20 μW/bit in [3]) tunneling-based SRAM (TSRAM) gain cell using two transistors and two resonant-tunneling diodes (RTDs) [6]. The RTDs had asymmetric *I-V* characteristics (NDR in one bias direction only). For one-bit/cell storage, a static one-transistor (1-T) TSRAM cell design similar to a DRAM cell yields the highest bit density. In this paper, we outline the layout and fabrication of an ultra-compact single transistor low power TSRAM cell and also analyze the current-voltage (I-V) characteristics of low current density RTDs.

This cell concept also applies to silicon if a low current density Si-based NDR device is available. It would eliminate the power waste associated with the refresh operation [6]—a serious problem for the gigabit era [7]. Alternatively, TSRAM could allow relaxation of transistor leakage requirements and an increase in transistor current drive, i.e. higher read/write speed.

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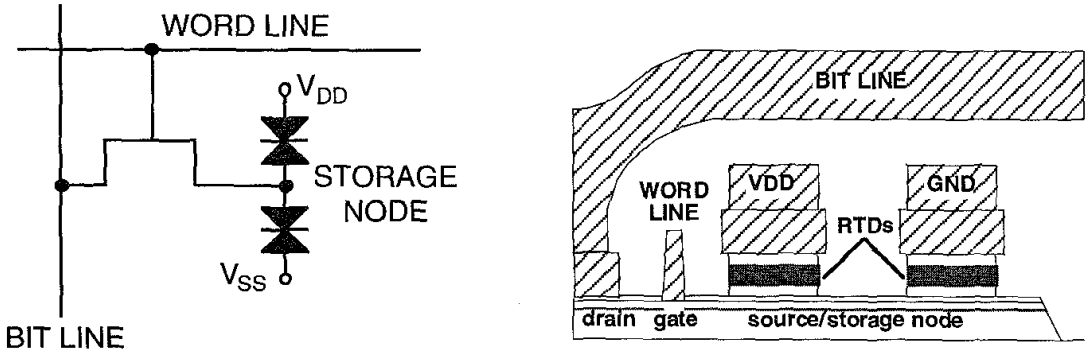
2. One-Transistor TSRAM Cell

To achieve the most compact one-transistor cell symmetric *I-V* RTDs are used. Asymmetric RTDs require a metal interconnect to tie one RTD emitter to the other RTD collector. The symmetric RTDs we have developed allow current to flow top-down in one RTD to the storage node and then bottom-up through the other RTD, see Figure 1. Both RTDs sit on an HFET source region, which is the storage node, to form a 1-T TSRAM cell with a shared bit line contact. Figure 2 shows a layout with only $2^1/_2$ via contacts versus $3^1/_2$ for a cell using asymmetric RTDs and achieving 4x smaller size than 6-transistor cells at the same design rule. The cell is read like a DRAM cell, the capacitance of the RTDs driving the bit line. Therefore, peak-minus-valley RTD currents need only be larger than HFET leakage currents.

Figure 3 shows a photo of a fabricated 4 bit x 4 word TSRAM die. Tests and SPICE simulation on such arrays show that the cell charge can be sensed dynamically with subnanosecond access times. This results from high storage node capacitance of 8 fF per μm^2 RTD area and a reduced bit line length because of the compact cell size.



(a) (b)

Figure 1. One-transistor TSRAM cell with symmetric RTDs storing a bit on the source of an HFET: circuit (a) and schematic cross-section with self-aligned word line (b).

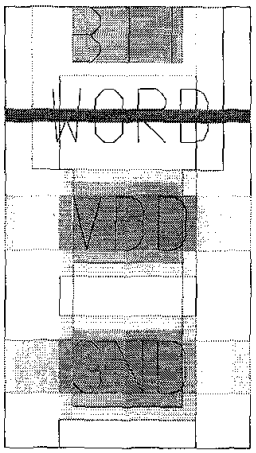


Figure 2. One-transistor TSRAM cell layout, 148.5 μm^2, at a relaxed 5 μm metal pitch.

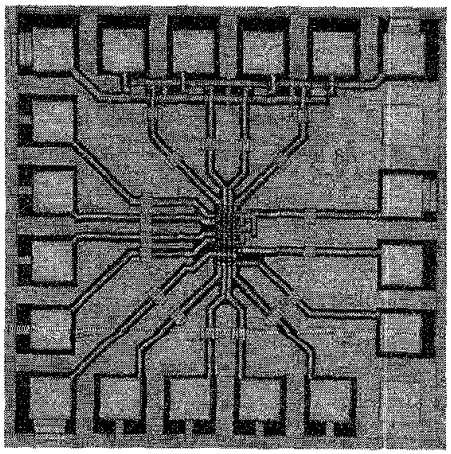


Figure 3. Fabricated 4x4 single-transistor cell TSRAM array.

3. Low Current Density RTDs

Figure 4 shows experimental *I-V* characteristics of several low current density RTDs for peak current densities ranging from 10 to about 0.1 A/cm^2. The low current density RTDs are modeled with our in-house developed nanoelelectronic simulator, NEMO [8]. An asymmetric RTD energy band diagram is shown in Figure 5, with a prebarrier for current reduction. A 10 band sp^{3}s* tightbinding model [8,9] including strained bandstructure parameters [10], full numerical integration of the current density over transverse momentum, full Hartree charge self-consistency [9,11], and strong electron-electron relaxation in the emitter region yield agreement with experiment. The coherent simulation uses incident electron energies up to 0.35 eV (~ 14 *kT*) to capture current flow through wide resonances up to 0.25 eV above the emitter Fermi level. Reduced prebarrier attenuation for the high energy wavefunctions contributing to the valley current causes a PVCR decrease for thicker prebarriers. This trend [12] together with HFET leakage impacts the ultimate reduction of TSRAM cell standby power. Figure 6 shows measured low temperature *I-V* characteristics for the 17 ml prebarrier structure and simulated curves reproducing the thermionic emission near the top of the prebarrier. Bandstructure dependence on temperature and phonon or roughness scattering in the central device region were neglected.

An improved symmetric RTD has been designed and fabricated with measured *I-V* characteristic shown in Figure 7. Details of the material structure will be reported at a later date, but the structure is near-ideal in the forward direction: a very small peak voltage combined with a wide (~ 1 V) valley region. A latch (Fig. 1) constructed of such RTDs has stable points far apart and close to the supply voltages.

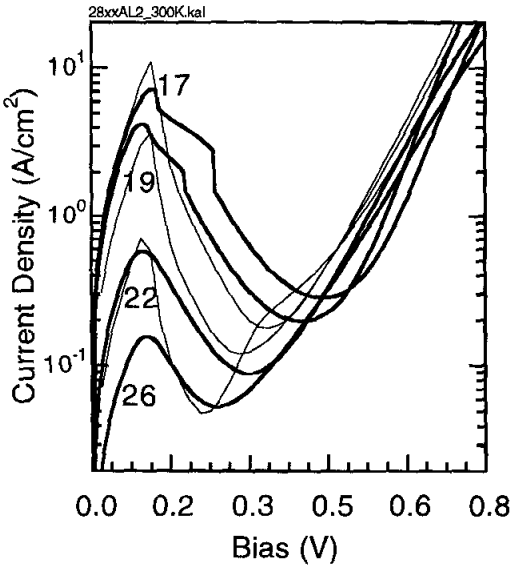


Figure 4. Room temperature experimental (thick) and theoretical (thin) I-V curves for asymmetric low current density RTDs of a design shown in Fig. 5. Numbers refer to prebarrier thickness in monolayers (1 ml = 2.93 Å).

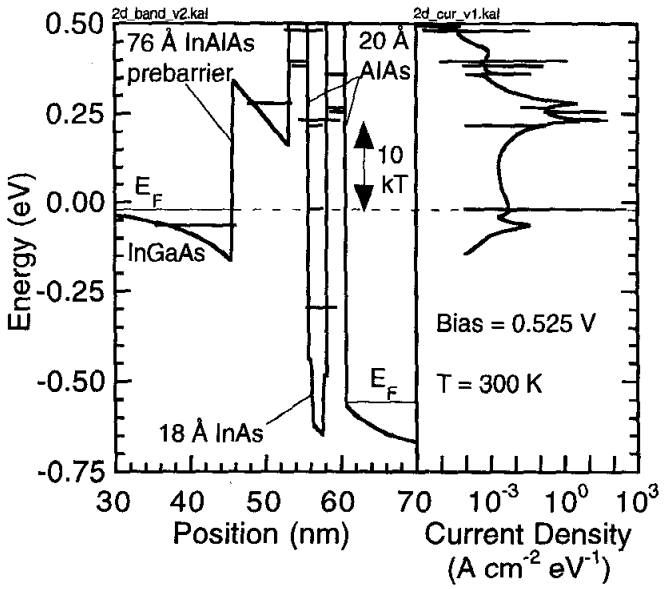


Figure 5. Conduction band diagram and current density of 26 ml prebarrier RTD biased in the valley region. Significant current flows through high energy wide resonances. The narrow resonances are due to multiband Γ-X transitions and carry negligible current. The current density units apply to a parabolic transverse energy-momentum band.

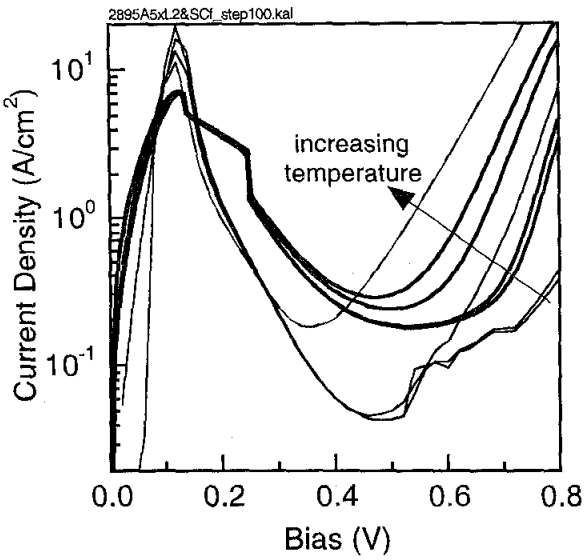


Figure 6. Experimental (thick) and theoretical (thin) I-V characteristics for an asymmetric 17 ml prebarrier RTD at 4, 100, 200, and 300 K.

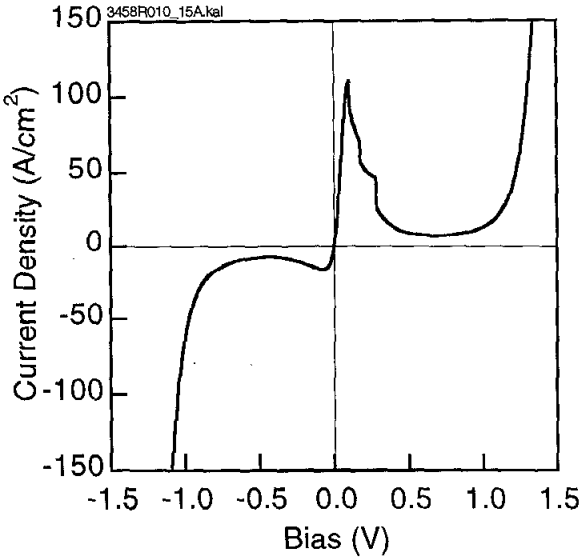


Figure 7. Room temperature experimental *I-V* curve for a symmetric low current density RTD. Asymmetry in growth causes the asymmetry in the *I-V*.

4. Conclusion

We have proposed and fabricated static memory cells using an ultracompact (150 μm^2) one-transistor tunneling-based SRAM cell. The cell uses two symmetric *I-V* low current density (~ 1 A/cm^2) RTDs and is capable of achieving nanowatt standby power per bit, which is orders of magnitude better than conventional 6-transistor cells. The valley current of the low current density RTDs was found to be caused in large part by thermionic electrons excited up to 0.25 eV (~ 10 *kT*) above the emitter Fermi level, which may cause the decreasing peak-to-valley current ratios toward lower current densities.

Acknowledgment

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